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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/005,627	12/04/2001	Nai-Shung Chang	JCLA6879	8225

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EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 12/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/005,627	CHANG ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 7 and 16 are objected to because of the following informalities: regarding claim 7, "one of he" on line 12 should be "one of the"; regarding claim 16, "an clock enable signal" should be "a clock enable signal". Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. Claim 6 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, Applicant fails to disclose how a switch with claimed terminals is able to control the connection between the termination resistor and the voltage source when the switch is located between the signal line [first terminal] and termination resistor [second terminal]. The Examiner submits that it would require undue experimentation for one of ordinary skill in the art to make and use the invention for the reason set forth hereinabove. To proceed with prosecution, Examiner will assume the switch is supposed to control the connection between the signal line and terminal resistor.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5, 7-13, 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan, US Patent 6665736, in view of Taguchi, US Patent 6480030.

5. In re claim 1, Fan discloses a motherboard [300], comprising [fig.3a]:

- A memory module slot [303] for connecting a memory module [305].
- A DDR (Double data rate) termination array [array of Rt's corresponding to signal lines; col.5, ll.1-22], coupled to the memory module slot for providing a plurality of termination resistors [array of Rt's] connected between a voltage source [Vtt] and the memory module slot [col.2, ll.18-43].
- A controller chip set [301], coupled to the memory module slot and the DDR termination array to provide a control signal [col.1, ll.28-40; 301 directs access to memory modules with control signals traveling through memory module slot to terminating Rt].

6. Fan did not discuss reducing power consumption.

7. Taguchi discloses a configuration with reduced power consumption [col.2, ll.50-54], comprising:

- A termination array [21, 22 with associated circuitries], wherein connections between the voltage source [Vtt] and the termination resistors [Rt] are controlled according to an indication of a control signal [col.5, ll.33-48].
- A controller chip set [inherently, a controller chip set in the broadest interpretation is needed to issue a control signal], wherein when the configuration enters a power saving mode [low speed mode], the control signal commands the termination array [21, 22] to cut off the connections between the termination resistors [Rt] and the voltage source [Vtt] [col.5, ll.33-48].

8. It would have been obvious to one of ordinary skill in the art, having the teachings of Fan and Taguchi before him at the time the invention was made, to modify the motherboard taught by Fan to include the teachings of Taguchi in order to obtain the claimed motherboard with reduced power consumption. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption [Taguchi: col.1, l.65 – col.2, l.11; col.2, l.50 – col.3, l.2; col.5, ll.33-48].

9. As to claims 2, 9 and 16, the Examiner hereby takes Official Notice that it is well known in the art to have a control signal that includes a clock enable signal.

10. As to claims 3 and 10, Fan discloses, wherein the memory module comprises a double data rate dynamic random access memory (DDR DRAM) [305; col.1, ll.41-67].

11. As to claims 4, 11 and 16, the Examiner hereby takes Official Notice that it is well known in the art to have a motherboard be used in a laptop computer.

12. As to claims 5 and 12, Fan discloses, wherein the controller chip set comprises a north bridge chip [301].

13. As to claim 7, Fan discloses the motherboard wherein the DDR termination array comprises a plurality of signal terminals [inherently, signal terminals in the broadest interpretation is needed in order to facilitate transfer of signals], coupled to a plurality of corresponding signal buses [signal lines corresponding to data bus of DIMM] [col.2, ll. 27-42; col.5, ll.10-22] while Taguchi discloses a switch [e.g., 21], comprising a first terminal [to Vtt], a second terminal [to Rt] and a control terminal [inherently, a control terminal in the broadest interpretation is needed to receive the control signal], the first terminal being connected to the voltage source and wherein each one of the termination resistors [Rt] is connected between one

of the signal terminals [on bus] and the second terminal of the switch [*resistances* Rt connect to the plurality of signal lines on bus 10], and the control terminal of the switch receives the control signal to turn the switch on or off according to an indication of the control signal [fig.2; col.5, ll.9-48].

14. In re claim 8, Fan discloses a motherboard [300], comprising [fig.3a]:

- A memory module slot [303] for connecting a memory module [305].
- A plurality of termination resistors [array of Rt's], each of the termination resistors comprises a first terminal [to 303] and a second terminal [to Vtt], wherein the first terminals of the termination resistors are coupled to the memory module slot [fig.3a; col.5, ll.1-22; col.2, ll.18-43].
- A controller chip set [301], coupled to the memory module slot to provide a control signal [col.1, ll.28-40; 301 directs access to memory modules with control signals traveling through memory module slot to terminating Rt].
- A DDR (Double data rate) termination array [array of Rt's corresponding to signal lines; col.5, ll.1-22], coupled to the memory module slot for providing a plurality of termination resistors [array of Rt's] connected between a voltage source [Vtt] and the memory module slot [col.2, ll.18-43].
- A controller chip set [301], coupled to the memory module slot and the DDR termination array to provide a control signal [col.1, ll.28-40; 301 directs access to memory modules with control signals traveling through memory module slot to terminating Rt].

15. While Taguchi discloses a configuration with reduced power consumption [col.2, ll.50-54], comprising:

- A plurality of termination resistors [*resistances* Rt connect to the plurality of signal lines on bus 10], each of the termination resistors comprises a first terminal [to bus 10] and a second terminal [to 21, 22] [fig.2; col.5, ll.9-48].
- A switch [21], comprising a first terminal [to Rt], a second terminal [to Vtt] and a control terminal [inherently, a control terminal in the broadest interpretation is needed to receive the control signal], wherein the second terminals of the termination resistors are coupled to the first terminal of the switch, the second terminal of the switch is coupled to a voltage source {Vtt], and the control terminal is used to receive a control signal [fig.2; col.5, ll.9-48].
- A controller chip set [23], coupled to the switch to provide the control signal [col.5, l.49 – col.6, l.41; 23 sends control signal to 32-34 representing the switches], wherein when the configuration enters a power saving mode [low speed mode] or when the memory module is not inserted in the memory module slot, the control signal commands the switch to cut off the connection between the termination resistors and the voltage source [col.5, ll.33-48].

16. In re claim 13, Fan discloses an operation method of a motherboard [300], wherein the motherboard comprises a memory module slot [303] and a plurality of termination resistors [array of Rt's], the termination resistors, the memory module slot and a voltage source [Vtt] form an operation circuit [fig.3a; col.5, ll.1-22; col.2, ll.18-43], the operation method comprising:

- Using a control signal [on] to establish the connection between the voltage source and the operation circuit when the motherboard enters a normal operation mode and when the

memory module slot is inserted with the memory module [motherboard operates normally when turned on with memory module in slot].

17. While Taguchi discloses an operation method of a configuration with reduced power consumption [col.2, ll.50-54], the operation method comprising [fig.2; col.5, ll.9-48]:

- Providing a control signal wherein a connection between a voltage source [Vtt] and an operation circuit [Rt, Vtt] is controlled by an indication of the control signal [open/close switch].
- Using the control signal to cut off the connection between the voltage source and the operation circuit when the configuration enters a power saving mode [low speed mode] [open switch].
- Using the control signal to establish the connection between the voltage source and the operation circuit when the configuration enters a normal operation mode [high speed mode] [close switch].

18. As to claim 15, Taguchi discloses, wherein the cutting off step comprises a step of cutting off connections between the termination resistors and the voltage source [fig.2; col.5, ll.33-48].

19. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan and Taguchi as applied to claims 1 and 13 above, and further in view of Wallace, US Patent 5635852.

20. In re claim 6, Fan and Taguchi disclose each and every limitation of the claim as discussed above in reference to claim 1. In particular, Fan discloses the motherboard wherein the DDR termination array comprises a plurality of signal terminals [inherently, signal terminals in the broadest interpretation is needed in order to facilitate transfer of signals], coupled to a

plurality of corresponding signal buses [signal lines corresponding to data bus of DIMM] [col.2, ll. 27-42; col.5, ll.10-22] while Taguchi discloses a plurality of switches [21, 22], wherein each of the switches comprises a first terminal, a second terminal and a control terminal [inherently, a control terminal in the broadest interpretation is needed to receive the control signal].

21. Fan and Taguchi did not discuss the particular details of a switch terminal connected to the signal terminal.

22. Wallace discloses a termination array [300] that comprises:

- A switch [404 with associated circuitries] that comprises a first terminal [to 706 or signal line], a second terminal and a control terminal [510], and each of the first terminals is connected to one of the signal terminals [706 to bus line 704] [fig.4].
- Wherein a control signal [enable 504] commands the switch [404] being switched on or off for controlling the connection between a termination resistor [740] and the signal line [704] [col.4, l.40 – col.5, l.17; col.6, ll.44-65].

23. It would have been obvious to one of ordinary skill in the art, having the teachings of Wallace, Fan and Taguchi before him at the time the invention was made, to modify the motherboard taught by Fan and Taguchi to include the teachings of Wallace in order to obtain the claimed motherboard with reduced power consumption. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption [Taguchi: col.1, l.65 – col.2, l.11; col.2, l.50 – col.3, l.2; col.5, ll.33-48; Wallace: col.6, ll.44-65].

24. In re claim 14, Fan and Taguchi disclose each and every limitation of the claim as discussed above in reference to claim 13. Fan and Taguchi did not discuss cutting off connection between the resistors and the memory module slot.

25. Wallace discloses the operation wherein the cutting off step comprises a step of cutting off connections between the termination resistor [740] and the slot [cell 700] [col.4, l.40 – col.5, l.17; col.6, ll.44-65].

26. It would have been obvious to one of ordinary skill in the art, having the teachings of Wallace, Fan and Taguchi before him at the time the invention was made, to modify the motherboard taught by Fan and Taguchi to include the teachings of Wallace in order to obtain the operation wherein the cutting off step comprises a step of cutting off connections between the termination resistors and the memory module slot. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption [Taguchi: col.1, l.65 – col.2, l.11; col.2, l.50 – col.3, l.2; col.5, ll.33-48; Wallace: col.6, ll.44-65].

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited U.S. patent documents describe various systems and methods associated with terminators as well as various well known concepts in the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
December 21, 2004

REHANA PERVEEN
PRIMARY EXAMINER